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John D. Cowart
NCR Corporation
Law Department IP WHQ-4W
1700 S. Patterson Blvd.
Dayton, OH 45479

EXAMINER

PATEL, ISHWARBHAI B

ART UNIT	PAPER NUMBER
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2841

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/670,829

Applicant(s)

FAN ET AL.

Examiner

Ishwar (I. B.) Patel

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 June 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) 11, 12 and 20-26 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 13-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 9/25/03 & 2/18/04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of group I, specie A1B3, claims 1-10 and 13-19 in the reply filed on June 22, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Regarding the statement "the office failed to define species for figure 5, which has readable claims", it was clarified with applicant representative Harden E. Steve, on July 1, 2005, that specie on figure 5 were considered but by mistake figure number 4 was referred, instead of figure 5 against A2, in the restriction requirements. As that specie was not elected, it does not have any effect on the elected specie.

Claim Objections

2. Claims 1-10 and 13-19 are objected to because of the following:

Regarding claim 1, the phrase "wherein the first and second decoupling capacitors are aligned generally along the direction to increase an amount of space in the circuit board through which the vias are extendable" is unclear. In particular "(to) increase an amount of space in the circuit board through which the vias are extendable" does not make it clear what space the applicant is talking about. For the examination purpose it was assumed that the vias referred to are those vias beyond the periphery of the decoupling capacitors.

Claims 2-10 depend upon claim 1 and inherit same deficiency.

Regarding claim 13 and 14: In claim 13, The phrase "wherein each pair of the first and second decoupling capacitors are aligned generally along a direction that is generally perpendicular to a main surface of the circuit board to increase an amount of space in the circuit board for vias that are extendable through the first and second reference plane layers" is misleading. The decoupling capacitors are aligned to increase the distance between the vias, but the vias are not positively claimed. Also, claim 14, which depend upon claim 13, is reciting "the vias", but vias are not claimed in claim 13, and thus lacks antecedent basis. For the examination purpose, there assumed to be vias beyond the periphery of the decoupling capacitors, other than those connected with the capacitors.

Claims 14-19 depend upon claim 13 and inherit same deficiency.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blakely et al., US Patent No. 6,618,266 in view of Ehman et al., US Patent No. 6,021,050 and Chakravorty, US Patent No. 6,611,419.

Regarding claim 1, Blakely et al., in figure 3-6, discloses a circuit board comprising: first (102c) and second reference plane (102d) layers; a first decoupling capacitor (104a) mounted to a surface of the first reference plane layer (102c); a second decoupling capacitor (104c) mounted to a surface of the second reference plane layer (102d).

Blakely et al., further discloses vias extending generally along a direction through the first and second reference plane layers, wherein the first and second decoupling capacitors are aligned generally along the direction.

Blakely et al., does not disclose the vias beyond the periphery of the decoupling capacitors, other than those connected with the capacitors.

Ehman et al., in figure 1, discloses a circuit board with two pairs of embedded capacitors (48 and 54) on one layer and another pair (48 and 54) on another layer and through vias (56) passing through the circuit board. As can be seen, the positioning of the capacitors one above the other will provide the better routing of the through vias. Ehman et al., further discloses components (58) and (60) mounted on the surface, which can be any component, passive or active, (column 5, line 43-50).

Chakravorty, in figure 4, discloses an electronic assembly with capacitors (430, 440) with through vias (one (409) shown in figure), with a semiconductor die (400) mounted on the upper surface of the board.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Blakely et al., with vias beyond the periphery of the decoupling capacitors, other than those connected with the

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capacitors, as taught by Ehman et al., and Chakravorty, in order to facilitate better routing of the through vias.

Regarding claim 2, the modified assembly of Blakely et al., further discloses the vias comprise through-hole vias that extend from one side of the circuit to another side of the circuit board, as applied to claim 1 above.

Regarding claim 3, the modified assembly of Blakely et al., further discloses additional first decoupling capacitors (104b) mounted to the surface of the first reference plane layer, and additional second decoupling capacitors (104d) mounted to the surface of the second reference plane layer, wherein each pair of first and second decoupling capacitors are aligned generally along the direction such that multiple spaced-apart lines of decoupling capacitors are provided, each line of decoupling capacitors including a respective pair of first and second decoupling capacitors.

Regarding claim 4, the modified assembly of Blakely et al., further discloses the vias extend through the circuit board in regions devoid of decoupling capacitors, (as applied to claim 1 above, shown by Ehman et al.).

Regarding claim 5, the modified assembly of Blakely et al., further discloses a dielectric layer (dielectric layer between layer 102c and 102d, Blakely et al., figure 6) between the first and second reference plane layers, wherein the first and second

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decoupling capacitors are separated by at least the first and second reference plane layers and the dielectric layer, and the vias extend through the first and second reference plane layers and the dielectric layer.

Regarding claim 6, the modified assembly of Blakely et al., further discloses each of the first decoupling capacitors includes a first electrode (107a) and a second electrode (106a), the circuit board further comprising a first buried via (110d) electrically contacted to the first electrode (107a) of one of the first decoupling capacitors, the first buried via extending through the first reference plane layer and the dielectric layer to electrically contact the second reference plane layer (see Blakely et al., figure 3-5, column 3, line 61 to column 4, line 10).

Regarding claim 7, the modified assembly of Blakely et al., further discloses each of the second decoupling capacitors (104c) includes first (106c) and second (107c) electrodes, the circuit board further comprising a second buried via (110c) electrically contacted to the first electrode (106c) of one of the second decoupling capacitors, the second buried via extending through the second reference plane layer and dielectric layer to electrically contact the first reference plane layer (see Blakely et al., figure 3-5, column 3, line 61 to column 4, line 10).

Regarding claim 8, the modified assembly of Blakely et al., further discloses

layers provided above and below a core assembly including the first and second reference plane layers, dielectric layer, and first and second decoupling capacitors (as shown by Ehman et al., in figure 1 and Chakravorty, in figure 4).

Regarding claim 9, the modified assembly of Blakely et al., further discloses the first decoupling capacitors are spaced apart with respect to each other across the surface of the first reference plane layer, and the second decoupling capacitors are spaced apart with respect to each other across a surface of the second reference plane layer (Blakely et al., figure 3 and Ehman et al., in figure 1).

Regarding claim 10, the modified assembly of Blakely et al., further discloses first regions between the spaced apart first decoupling capacitors (region between the capacitors 104a and 104b, Blakely et al., figure 3); and second regions between the spaced apart second decoupling capacitors (region between capacitors 104c and 104 d, Blakely et al., figure 3), the first and second regions being generally aligned along the direction, the vias extending through the circuit board through the first and second regions, (see figure 3).

Regarding claim 13, Blakely et al., in figure 3-6, discloses a system comprising: a circuit board comprising: first (102c) and second 9102d) reference plane layers; first decoupling capacitors (104a, 104b) mounted to a surface of the first reference plane layer, the first decoupling capacitors being spaced apart across the surface of the

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first reference plane layer; second decoupling capacitors (104c, 104d) mounted to a surface of the second reference plane layer, the second decoupling capacitors being spaced apart across the surface of the second reference plane layer; and wherein each pair of the first and second decoupling capacitors are aligned generally along a direction that is generally perpendicular to a main surface of the circuit board (see figure 3).

Blakely et al., does not disclose a power supply, and

an integrated circuit device to be powered by the power supply and vias beyond the periphery of the decoupling capacitors, other than those connected with the capacitors. However, Blakely et al., discloses that the modern high-speed digital system comprise one or more integrated circuit package mounted of printed circuit board and the present invention is to increase the capacitor density and decreases the number of vias required for capacitor placement on a printed circuit board (column 1, line 5-45). This implies that there will be an integrated circuit mounted on the circuit board and also discloses vias extending generally along a direction through the first and second reference plane layers, wherein the first and second decoupling capacitors are aligned generally along the direction. Those vias are connected to the decoupling capacitors.

Ehman et al., in figure 1, discloses a circuit board with two pairs of embedded capacitors (48 and 54) on one layer and another pair (48 and 54) on another layer and through vias (56) passing through the circuit board. As can be seen, the positioning of the capacitors one above the other will provide the better routing of the through vias.

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Ehman et al., further discloses components (58) and (60) mounted on the surface, which can be any component, passive or active, column 5, line 43-50.

Chakravorty, in figure 4, discloses an electronic assembly with capacitors (430, 440) with through vias (one (409) shown in figure), with a semiconductor die (400) mounted on the upper surface of the board.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to construe an integrated circuit mounted on the printed circuit board of Blakely et al., as taught by Ehman et al., and Chakravorty, in order to have the desired functionality of the system, vias beyond the periphery of the decoupling capacitors, other than those connected with the capacitors, to facilitate connection of other components.

Regarding the limitation "a power supply", though the modified system of Blakely et al., does not explicitly disclose a power supply, the power supply has to be there for operating the system.

Regarding claim 14, the modified assembly of Blakely et al., further discloses the vias comprise through-hole vias that extend from one side of the circuit board to another side of the circuit board, as applied to claim 13 above.

Regarding claim 15, the modified assembly of Blakely et al., further discloses

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the circuit board further comprises the vias, the vias extending through the circuit board in regions between spaced apart first and second decoupling capacitors (see Ehman et al., figure 1).

Regarding claim 16, the modified assembly of Blakely et al., further discloses the circuit board further comprises a dielectric layer (dielectric layer between layer 102c and 102d, Blakely et al., figure 6) between the first and second reference plane layers, wherein each of the first decoupling capacitors includes a first electrode (107a, 107b) and a second electrode (106a, 106b), and wherein the circuit board further comprises a first buried via (110d) electrically contacted to the first electrode of one of the decoupling capacitors, the first buried via extending through the first reference plane layer and the dielectric layer to electrically contact the second reference plane layer (see Blakely et al., figure 3-5, column 3, line 61 to column 4, line 10).

Regarding claim 17, the modified assembly of Blakely et al., further discloses each of the second decoupling capacitors (104c) includes first (106c) and second (107c) electrodes, wherein the circuit board further comprises a second buried via (110c) electrically contacted to the first electrode of one of the second decoupling capacitors, the second buried via extending through the second reference plane layer and dielectric layer to electrically contact the first reference plane layer (see Blakely et al., figure 3-5, column 3, line 61 to column 4, line 10).

Regarding claim 18, the modified assembly of Blakely et al., further discloses the circuit board further comprises layers provided above and below a core assembly including the first and second reference plane layers, dielectric layer, and first and second decoupling capacitors (as shown by Ehman et al., in figure 1 and Chakravorty, in figure 4).

Regarding claim 19, the modified assembly of Blakely et al., further discloses first regions between the spaced apart first decoupling capacitors (region between the capacitors 104a and 104b, Blakely et al., figure 3); and second regions between the spaced apart second decoupling capacitors (region between capacitors 104c and 104 d, Blakely et al., figure 3), the first and second regions being generally aligned along the direction, the vias extending through the circuit board through the first and second region (see figure 3).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hailey et al. US Patent No. 6,337,798, in figure 2, discloses decoupling capacitors C1 and C2, aligned in the direction of via holes.

Mamada, US Patent No. 6,304,425, in figure 2, discloses capacitors 1A and 1B, aligned in the direction of via holes.

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Gochi et al., US Patent No. 5,583,748, in figure 1, discloses two pairs of capacitors (4) aligned in the direction perpendicular to the surface of the circuit board.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Ishwar (I. B.) Patel

Examiner

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July 25, 2005